

FIG.1

CIRCUIT BLOCK DIAGRAM OF FIRST EMBODIMENT

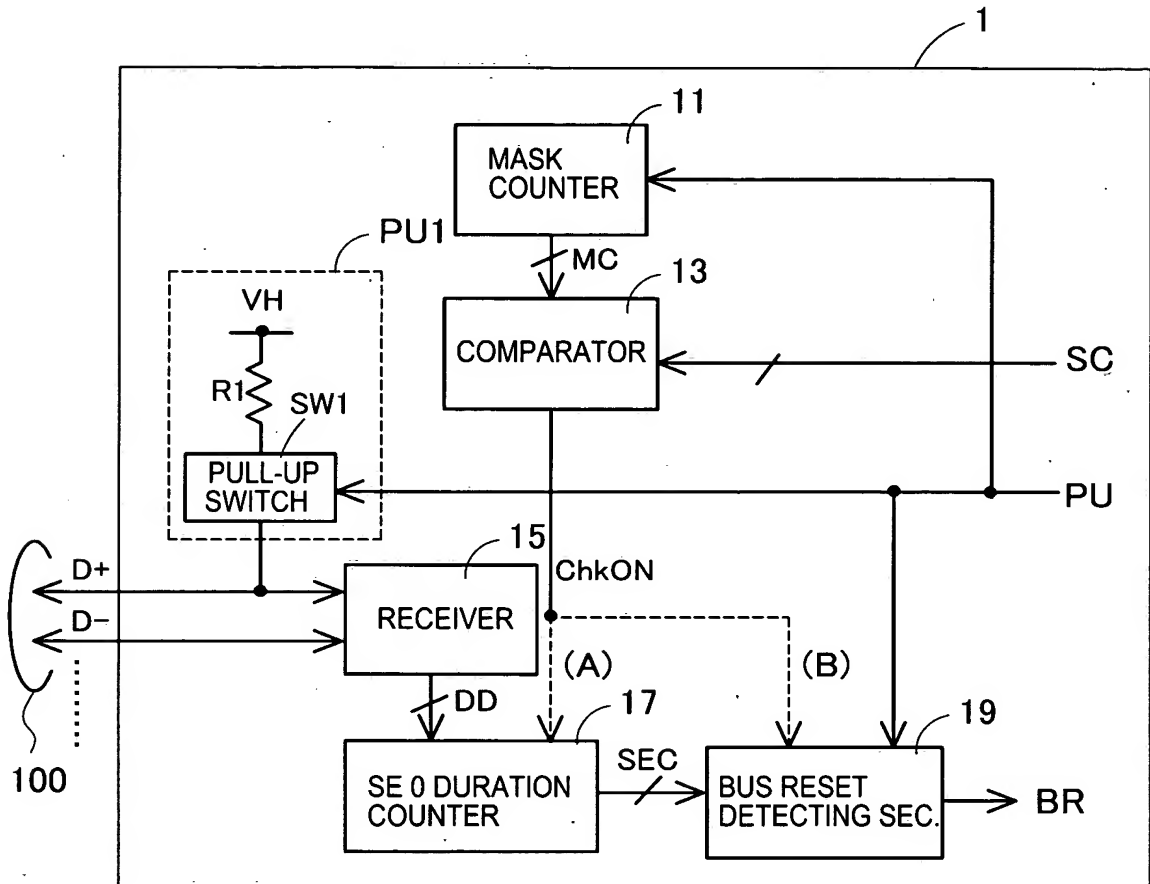


FIG.2
OPERATIONAL WAVEFORM OF FIRST EMBODIMENT

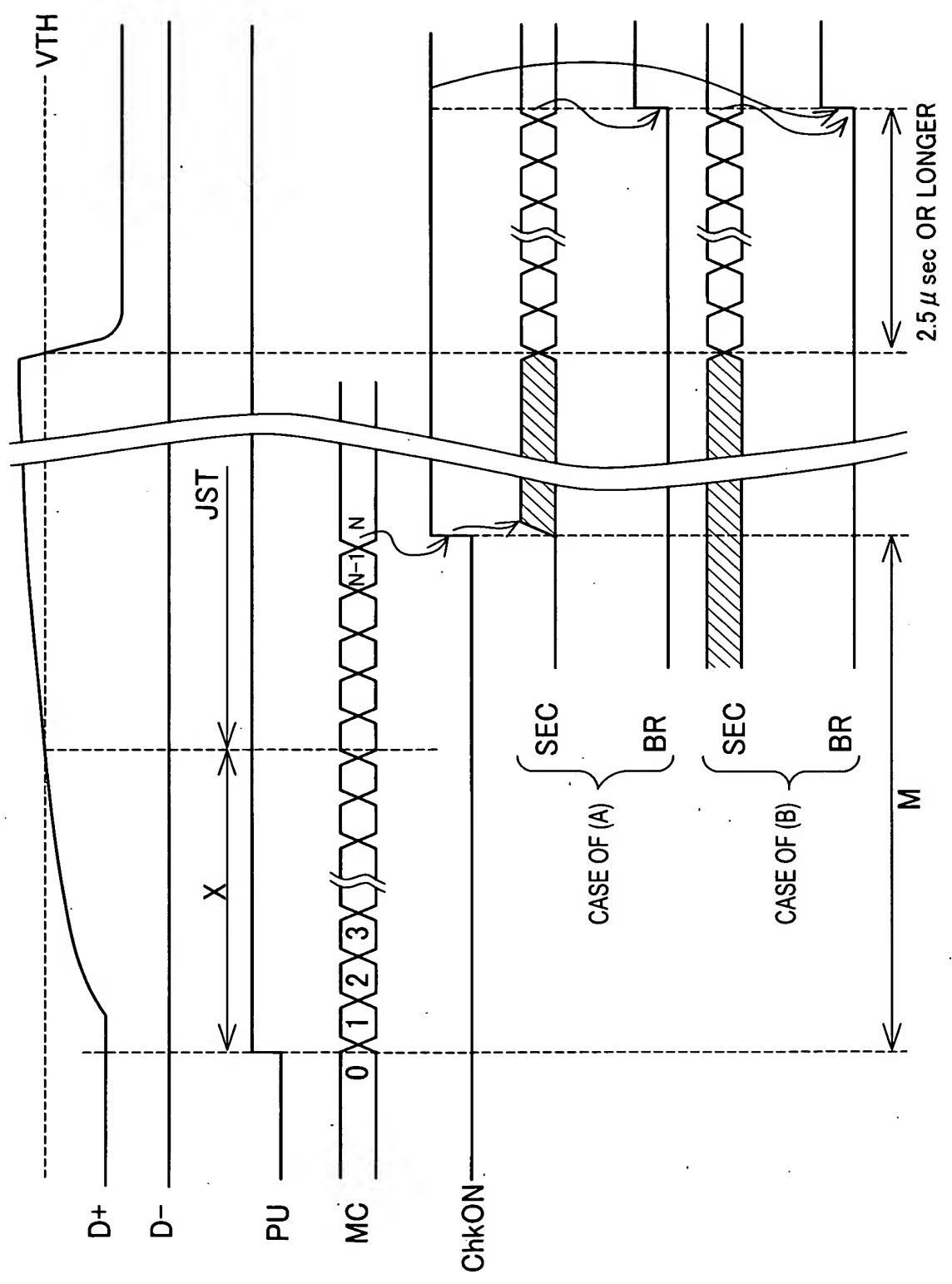


FIG.3

CIRCUIT BLOCK DIAGRAM OF SECOND EMBODIMENT

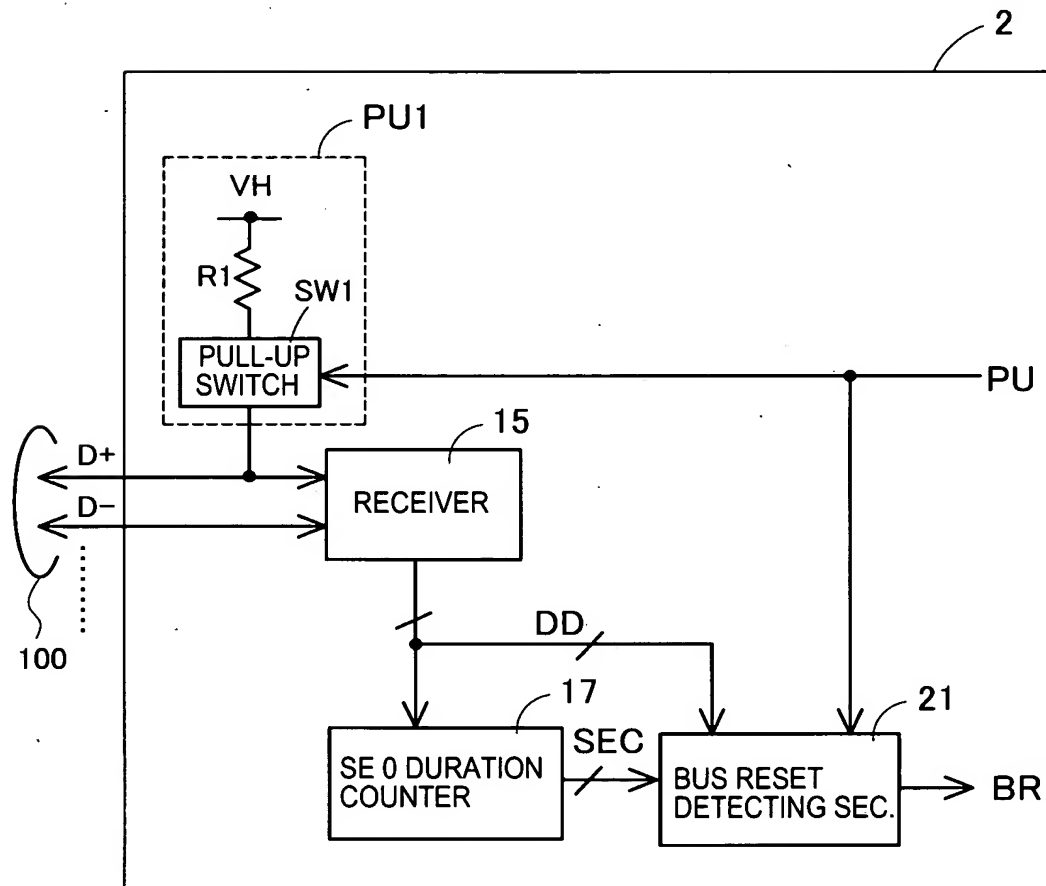


FIG.4
OPERATIONAL WAVEFORM OF SECOND EMBODIMENT

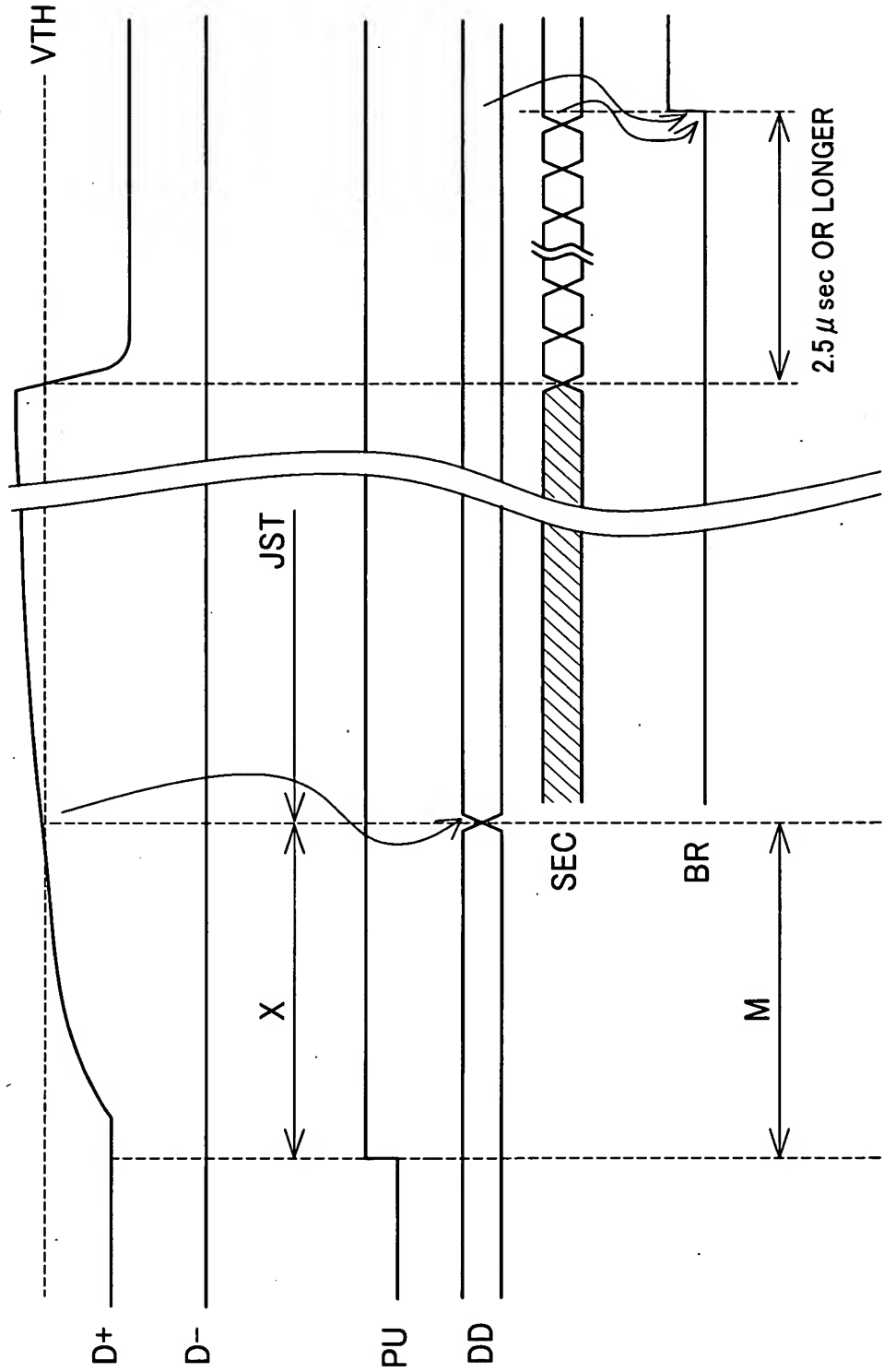


FIG.5

TERMINATION CIRCUIT OF UNIVERSAL SERIAL BUS

